

AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory

5 behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

thereafter simulating said built-in self-test circuit

10 and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address

15 patterns, and wherein said input address and data and said memory address and data are compared in said built-in self-

test circuit and a fault output is generated if not matching;

de-scrambling said set of faults; and

20 comparing said fault output and said de-scrambled set of faults to verify the performance of said built-in self-test circuit.

2. (Original) The method according to Claim 1 wherein said set of faults comprises an expected faults database file.

3. (Original) The method according to Claim 1 wherein said high level language comprises one of the group of: VHDL and Verilog.

4. (Original) The method according to Claim 1 wherein said set of faults comprise any of the group of: stuck at zero and stuck at one.

5. (Original) The method according to Claim 1 wherein said built in self-test circuit performs any algorithm of the group comprising: March C+, Checkerboard, March A, March B, Diagonal, and Walking 0/1.

6. (Original) The method according to Claim 1 wherein said

step of simulating further comprises:

scrambling said input data and address patterns prior to input into said embedded memory behavior model; and

5 de-scrambling said memory address and data prior to said comparing of said input address and data and said memory address and data in said built-in self-test circuit.

7. (Canceled)

8. (Currently Amended) A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

5 introducing a set of faults into an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

10 thereafter simulating said built-in self-test circuit and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein said input data and address patterns are scrambled prior to input into said embedded memory behavior model, wherein

15 said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are de-scrambled and then are compared to said input address and data in said built-in self-test circuit and a fault 20 output is generated if not matching; de-scrambling said set of faults; and thereafter comparing said fault output and said de-scrambled set of faults to verify the performance of said built-in self-test circuit.

9. (Original) The method according to Claim 8 wherein said set of faults comprises an expected faults database file.

10. (Original) The method according to Claim 8 wherein said high-level language comprises one of the group of: VHDL and Verilog.

11. (Original) The method according to Claim 8 wherein said set of faults comprise any of the group of: stuck at zero and stuck at one.

12. (Original) The method according to Claim 8 wherein

said built-in self-test circuit performs any algorithm of the group comprising: March C+, Checkerboard, March A, March B, Diagonal, and Walking 0/1.

13. (Currently Amended) An apparatus to verify the performance of a built-in self test circuit for testing embedded memory in an integrated circuit device comprising:

 an embedded memory behavior model wherein said
5 embedded memory behavior model comprises a high-level language model;

 a built-in self-test circuit model connected to said embedded memory behavior model wherein said built-in self-test circuit model generates input data and address
10 patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are compared to said input address and data in said built-in
15 self-test circuit and a fault output is generated if not matching;

 a means of introducing a set of faults into said embedded memory behavior model wherein each member of said set of faults comprises a finite state machine state, a
20 memory address, and a memory data fault;

a means of simulating said embedded memory behavior
 model and said built-in self-test circuit model;
 a means of de-scrambling said set of faults; and
 a means of comparing the fault ~~diagnosis~~ output
25 of said built-in self-test circuit model and said
 de-scrambled set of faults to verify the performance of
 said built-in self-test circuit.

14. (Original) The apparatus according to Claim 13 wherein
 said set of faults comprises an expected faults database
 file.

15. (Original) The apparatus according to Claim 13 wherein
 said high-level language comprises one of the group of:
 VHDL and Verilog.

16. (Original) The apparatus according to Claim 13 wherein
 said set of faults comprise any of the group of: stuck at
 zero and stuck at one.

17. (Original) The apparatus according to Claim 13 wherein
 said built-in self-test circuit model performs any
 algorithm of the group comprising: March C+, Checkerboard,
 March A, March B, Diagonal, and Walking

18. (Original) The apparatus according to Claim 13 further comprising:

a means of scrambling said input data and address patterns prior to input into said embedded memory

5 behavior model; and

a means of de-scrambling said memory address and data prior to said comparing of said input address and data and said memory address and data in said built-in self-test circuit.

19. (Canceled)

20. (Original) The apparatus according to Claim 13 wherein said built-in self-test circuit model comprises a register transfer level or gate level design.